REMARKS

The indication of allowable subject matter in claims 3 and 14 is acknowledged and appreciated. In view of the following remarks, it is respectfully submitted that all claims are in condition for allowance.

Claims 1 and 13 are the sole rejected independent claims and stand rejected under 35 U.S.C. § 103 as being unpatentable over Dreifus '621 ("Dreifus") in view of newly cited Kato et al. '821 ("Kato"). This rejection is respectfully traversed for at least the following reasons.

In order to expedite prosecution, Applicants' representative initiated a telephone interview with Examiner Koyama to discuss the merits of the claimed invention. Applicants and Applicants' representative would like to thank Examiner Koyama for her courtesy in conducting the interview and for her assistance in resolving issues. As a result of the interview, the Examiner agreed that the pending rejection was improper and would be withdrawn, placing the application in condition for allowance pending an updated prior art search. A summary of the interview follows.

Claim 1 recites in pertinent part, "state control means for halting the write and read processing on said ***buffer memory*** and said ***nonvolatile memory*** of said CPU while said transmission circuit is sending/receiving data to/from the outside" (emphasis added; claim 13 is submitted to be patentable for at least reasons similar to those that will be discussed below with respect to claim 1). The Examiner admits that Dreifus does not disclose or suggest the claimed functionality of the state control means and therefore relies on Kato to modify Dreifus in an attempt to obviate this deficiency of Dreifus. However, it is respectfully submitted that even

assuming *arguendo* proper, the proposed combination does not disclose or suggest the claimed combination.

As noted by the Examiner, access from the CPU 808 ***to the data storage memory 804*** is halted when the data storage memory 804 is accessed by the external computer apparatus 812. However, access to the ***alleged nonvolatile memory*** is NOT halted. Indeed, the device of Kato can read programs stored in the ROM 802 even while the switching control circuit halts access from the CPU 808 *to the alleged buffer memory 804*. Kato is completely silent as to halting the write and read processing on the alleged non-volatile memory. As discussed during the interview, Kato is silent as to the configuration of storage memory 804, let alone suggest that it can be a ***non-volatile*** memory. Moreover, it is respectfully submitted that one of ordinary skill in the art, without express disclosure stating otherwise, would interpret storage memory 804 as a conventional ***buffer*** memory in view of the data ***transfer*** thereto rather than the typical program storage (e.g., permanent storage, etc.) of a non-volatile memory. In any event, Kato discloses only, at best, halting operation on one type of memory (storage memory 804; i.e., buffer); but is completely silent as to halting operations on both a ***buffer memory*** and ***nonvolatile memory***.

In view of the foregoing, it is respectfully submitted that neither Dreifus nor Kato, alone or in combination, disclose or suggest "halting the write and read processing ***on said buffer memory and said nonvolatile memory of said CPU*** while said transmission circuit is sending/receiving data to/from the outside" as recited in claim 1 (similarly in claim 13). The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in claims 1 and 13 because the proposed combination fails the "all the claim limitations" standard required under § 103.

One of the objects of present invention is to enable halting read and write processing on a buffer memory or a nonvolatile memory by a central processing unit (CPU) while a transmission circuit is sending/receiving data to/from the outside. Accordingly, the influence of noise on the transmission circuit caused by operations of the nonvolatile memory and the CPU can be suppressed, whereby reliability in the send/receive processing can be increased.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination. Based on the foregoing, it is submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 103 be withdrawn.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 103 be withdrawn.

CONCLUSION

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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